METHOD FOR PROGRAMMING P-CHANNEL EEPROM

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 92133507, filed November 28, 2003.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method for operating a semiconductor device. More particularly, the present invention relates to a method for programming a P-channel electrical erasable programmable read-only memory (EEPROM).

Description of the Related Art

[0002] Electrical erasable programmable read-only memory (EEPROM) is a type of non-volatile memory with many advantages including a rapid response, a large storage capacity and a small size. Hence, EEPROM has become one of the most frequently used portable memory devices. Earlier EEPROM was constructed of N-type transistors and programmed with channel hot electron injection (CHEI). However, the CHEI programming method has low electron injection efficiency. Hence, newer EEPROM is constructed of P-channel transistors and programmed with band-to-band tunneling hot electron injection (BTBTHEI). The BTBTHEI method has an electron injection efficiency roughly two magnitudes higher than that of the CHEI method, and hence makes a much higher programming speed.

[0003] Fig. 1 is a schematic cross-sectional view of a P-channel EEPROM undergoing a programming operation using a conventional BTBTHEI method. The P-channel EEPROM comprises an N-well 100, a floating gate 110, a control gate 120, a select gate 130, a P-type source region 140, a P-type drain region 150 and a P-doped region 160 coupled to a bit line (not shown). To program the P-channel EEPROM, a negative voltage V_d is applied to the bit line/P-doped region 160, and another negative voltage V_{sg} is applied to the select gate 130 to turn on the channel below so that the negative voltage is passed to the drain region 150. In the meantime, a high positive voltage V_{cg} is applied to the control gate 120 to induce band-to-band tunneling hot electrons under the floating gate 110 close to the drain region 150, and a part of the hot electrons are attracted into the floating gate 110. Furthermore, the source region 140 is floated in the conventional BTBTHEI method.

[0004] However, both the CHEI programming method for N-channel EEPROM and the BTBTHEI programming method for P-channel EEPROM need relatively high operation voltages. Fig. 3 is a graph showing the variation of threshold voltage of a memory cell with time at different bit line voltage V_d using the conventional BTBTHEI method for programming a P-channel EEPROM. As shown in Fig. 3, the control gate voltage V_{cg} is set to a constant voltage of 7V. To generate sufficient band-to-band tunneling hot electrons so that programming can be completed within a designated period, a negative voltage V_d up to –7V, rather than –5V or –3V, must be applied to the bit line. With the application of such a high negative voltage, reducing the channel length of the select gate 130 is unfeasible due to the possibility of an increase in punch-through leakage.

[0005] Furthermore, to increase the amount of hot electrons and the percentage of injected hot electrons for speeding up the programming operation, usually a negative

voltage V_{sg} up to –8V to –9V is applied to the select gate 130, and a positive voltage V_{cg} up to 8V to 9V is applied to the control gate 120. Hence, the overall power consumption during a memory programming operation is relatively high in the prior art.

SUMMARY OF THE INVENTION

[0006] Accordingly, at least one object of the present invention is to provide a method for programming a P-channel electrical erasable programmable read-only memory (EEPROM). The method utilizes the snapback effect of a parasitic bipolar junction transistor (BJT) constituted of the source, the drain and the N-well to produce a large amount of hot electrons, so as to increase the efficiency of band-to-band tunneling hot electron injection (BTBTHEI).

[0007] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a P-channel EEPROM programming method. Instead of floating the source region, the method applies a positive voltage or a programming current to the source region. The forward bias such created is large enough to turn on a parasitic bipolar junction transistor (BJT) constituted of the source region, the drain region and the N-well. In addition, the N-well is grounded, a positive voltage is applied to the control gate and a negative voltage is applied to the drain region. The reverse bias resulting from the negative voltage generates a large electron current between the source region and the drain region, and some electrons are injected into the floating gate.

[0008] By utilizing the snapback effect of the parasitic bipolar junction transistor inside the EEPROM, a large amount of hot electrons are produced. Therefore, the voltage applied to the bit line, the select gate and the control gate of an EEPROM cell can be

lowered to save electrical power. Furthermore, with reduction of the bit line voltage, the length of channel underneath the select gate can be reduced to increase the read-out current and facilitate the miniaturization of a dual transistor (2T) device. In addition, the degree of programming can be controlled by adjusting the magnitude of the programming source current. Because the magnitude of a current is easier to control, this invention is particularly suitable for programming a multi-level cell (MLC).

[0009] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0011] Fig. 1 is a schematic cross-sectional view of a P-channel EEPROM undergoing a programming operation using a conventional BTBTHEI method.

[0012] Fig. 2 is a schematic cross-sectional view of a P-channel EEPROM undergoing a programming operation utilizing the snapback effect of a parasitic bipolar junction transistor according to this invention.

[0013] Fig. 3 is a graph showing the variation of threshold voltage of a memory cell with time at different bit line voltage V_d but a fixed V_{cg} of 7V using the conventional BTBTHEI method for programming a P-channel EEPROM.

[0014] Fig. 4 is a graph showing the variation of threshold voltage of a memory cell with time at different bit line voltage V_d but a fixed V_{cg} of 7V using the method for programming a P-channel EEPROM according to this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0016] Fig. 2 is a schematic cross-sectional view of a P-channel EEPROM undergoing a programming operation utilizing the snapback effect of a parasitic bipolar junction transistor according to this invention. As shown in Fig. 2, the P-channel EEPROM comprises an N-well 100, a floating gate 110, a control gate 120, a select gate 130, a P-type source region 140, a P-type drain region 150 and a P-doped region 160 coupled to a bit line (not shown). In the programming operation, a positive voltage V_{cg} of, for example, 5V-6V is applied to the control gate 120, the N-well 100 is grounded (that is, the voltage V_b of the N-well is 0V), and a positive voltage or a programming current I_s is applied to the source region 140. The programming current I_s can be set to several nA to several μA, for example, depending on the application. It is noted that the programming current I_s can be adjusted to reach a balance point between power consumption and programming speed. In general, increasing the programming current I_s increases the programming speed, but adversely increases the power consumption. Conversely, although decreasing the programming current I_s decreases the programming speed, the overall power consumption can be reduced.

[0017] The forward bias produced by applying the positive voltage or the programming current I_s to the source region 140 is large enough to turn on the parasitic bipolar junction transistor (BJT) constituted of the source region 140, the drain region 150 and the N-well 100. The source region 140, the N-well 100 and the drain region 150 serve as an emitter, a base and a collector, respectively. In addition, a negative voltage V_d of, for example, –3V - –5V is applied to the bit line/P-doped region 160, and a negative voltage V_{sg} of, for example, –4V - –6V is applied to the select gate 130 to switch on the channel underneath the select gate 130 and thereby pass the negative voltage of the P-doped region 160 to the drain region 150. The reverse bias caused by the negative voltage is large enough to produce a large electron current between the source region 140 and the drain region 150. These electrons are accelerated by the high electric field at the junction depletion region of the drain region 150 to produce hot electrons. Through the attraction of the high positive voltage V_{cg} applied to the control gate 120, a portion of the hot electrons is injected into the floating gate 110.

[0018] With the aforementioned voltage configuration, the programming period is set at the order of ten microseconds. Table 1 below lists all the programming conditions for the conventional BTBTHEI programming method as well as the aforementioned programming method of this invention.

Table 1

	V_d	Source (V_s)	V_{cg}	V_{sg}	V_b	Program-ming period	Factor affecting programming speed
Convent-ional	–6V- –7V	Floated	8V-9V	–8V- –9V	0	~10μs	V_d
This invention	–3V- –5V	Forward biased	5V-6V	–4V- –6V	0	~10μs	I_s

[0019] Fig. 4 is a graph showing the variation of threshold voltage of a memory cell with time at different bit line voltage V_d using the method of programming a P-channel EEPROM according to this invention. A fixed voltage V_{cg} of 7V is used. As shown in Fig. 4, the effect of setting the voltage V_d to –3V already exceeds the effect of setting the voltage V_d to –5V in the conventional programming method. When V_d is set to –5V, the effect is similar to that of setting the voltage V_d to –7V in the conventional programming method. In other words, using the programming method of this invention permits the employment of lower bit line voltage V_d.

[0020] In addition, when the programming period is fixed, increasing (or decreasing) the source current I_s can increase (or decrease) the amount of hot electrons injected into the floating gate, and thereby increase (or decrease) the degree of the raise of the threshold voltage of the channel. In general, the source current I_s is easier to control than the bit line voltage V_d. Hence, when an adjusting mechanism capable of varying

the source current I_s is setup, the programming method of this invention can be used to program a multi-level cell (MLC) to a specific threshold voltage level.

[0021] Because this invention utilizes the snapback effect of the parasitic bipolar junction transistor inside the EEPROM, a large amount of hot electrons are produced. Therefore, the voltages applied to the bit line, the select gate and the control gate of an EEPROM cell can be lowered to save electrical power. Furthermore, with a reduction of the bit line voltage, the length of channel underneath the select gate can be reduced to increase the read-out current and facilitate the miniaturization of a dual transistor (2T) device. In addition, the degree of programming can be controlled by adjusting the magnitude of the programming source current. Because the magnitude of a current is easier to control, this invention is particularly suitable for programming a multi-level cell (MLC).

[0022] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.